Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A fabrication method for a gate structure, comprising:
forming a pad layer on a surface of a substrate;
forming a patterned first photoresist layer on the pad layer, wherein the patterned first photoresist layer comprises a first opening that exposes the pad layer;
forming a cross-linked surface layer at the surface of the first photoresist layer;
performing a rounding step for rounding a profile of the first photoresist layer;
removing the pad layer not covered by the first photoresist layer to expose the surface of the substrate;
forming a patterned second photoresist layer on the first photoresist layer, wherein the second photoresist layer comprises a second opening that exposes a part of the first photoresist layer and the surface of the substrate that is being exposed by the first photoresist layer;
performing a deposition step to form a conductive layer on the second photoresist layer, the first photoresist layer and the surface of the substrate, wherein a part of the conductive layer formed on the second photoresist layer is separated from a part of the conductive layer formed on the first photoresist layer and the surface of

the substrate; and

removing the first photoresist layer and the second photoresist layer, and concurring stripping the part of the conductive layer formed on the second photoresist layer.

[c2] 2. The method of claim 1, wherein forming the cross-linked surface layer on the surface of the first photoresist layer comprises performing an ultra-violet curing step.

[c3] 3. The method of claim 1, wherein the rounding step comprises performing an ion-milling step or a thermal flowing baking step.

[c4] 4. The method of claim 1, wherein the deposition step comprises performing an evaporation step, a sputtering step or an electroplating step.

[c5] 5. The method of claim 1, wherein before forming the first photoresist layer, the method further comprises forming an anti-reflection layer on a surface of the pad layer.

[c6] 6. The method of claim 1, wherein the pad layer is formed with a material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

[c7] 7. The method of claim 1, wherein a width of the second

opening that exposes the first photoresist layer and the substrate surface is at least two times a width of the first opening that exposes the substrate surface.

[c8] 8. The method of claim 1, wherein a sidewall of the second opening and a sidewall of the first opening form an acute angle.

[c9] 9. The method of claim 1, wherein a wavelength of an exposure light source used in the patterning of the first photoresist layer is 436nm, 365nm, 248 nm or 193 nm.

[c10] 10. A fabrication method for a field effect transistor, the method comprising:
forming a pad layer on a surface of a substrate;
forming a patterned first photoresist layer on the pad layer, wherein the patterned first photoresist layer comprises a first opening that exposes the pad layer;
forming a cross-linked surface layer on a surface of the first photoresist layer;
performing a rounding process for rounding a profile of the first photoresist layer;
removing the pad layer not covered by the first photoresist layer to expose the surface of the substrate;
forming a patterned second photoresist layer on the first photoresist layer, wherein the second photoresist layer comprises a second opening that exposes the substrate

surface being exposed by the first photoresist layer and a part of the first photoresist layer;

performing a metal deposition step to form a metal layer on the second photoresist layer, the first photoresist layer and the surface of the substrate, wherein a part of the metal layer formed on the second photoresist layer is separated from a part of the metal layer formed on the first photoresist layer and the surface of the substrate;

removing the first photoresist layer, the second photoresist layer, and concurrently stripping the part of metal layer on the second photoresist layer, leaving the part of the metal layer formed on the surface of the substrate as a gate;

patterning the pad layer to expose the surface of the substrate; and

forming a source/drain region on the surface of the substrate.

[c11] 11. The method of claim 10, wherein forming the cross-linked surface layer on the surface of the first photoresist layer comprises performing an ultra-violet curing step.

[c12] 12. The method of claim 10, wherein the rounding step comprises performing an ion-milling step or a thermal flowing baking step.

[c13] 13. The method of claim 10, wherein the metal deposition step comprises a metal evaporation step, a metal sputtering step or a metal electroplating step.

[c14] 14. The method of claim 10, wherein before forming the first photoresist layer, the method further comprises forming an anti-reflection layer on a surface of the pad layer.

[c15] 15. The method of claim 10, wherein the pad layer is formed with a material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

[c16] 16. The method of claim 10, wherein a width of the second opening that exposes the first photoresist layer and the substrate surface is at least two times a width of the first opening that exposes the substrate surface.

[c17] 17. The method of claim 10, wherein a sidewall of the second opening and a sidewall of the first opening form an acute angel.

[c18] 18. The method of claim 10, wherein a material in forming the source/drain region comprises a metal material.

[c19] 19. The method of claim 10, wherein a wavelength of an exposure light source used in the patterning of the first photoresist layer is 436nm, 365nm, 248 nm or 193 nm.